NANOWIRE FET HAVING INDUCED RADIAL STRAIN

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of and claims the benefit of priority to U.S. application Ser. No. 12/631,203, now allowed, which was filed on Dec. 4, 2009. The entire contents of U.S. application Ser. No. 12/631,203 are incorporated herein by reference.

BACKGROUND

Aspects of the present invention are directed to a nanowire field effect transistor (FET) and, more particularly, to a nanowire FET with a metal gate that is surrounded with silicide around the metal gate for inducing radial and, in some cases, longitudinal strain in the nanowire channel.

In a field effect transistor (FET) with nanowire channels, it is possible to induce longitudinal strain in the nanowires since the relatively small diameters of the nanowires leads to efficient strain coupling from a stressor. While longitudinal strain was studied in detail in planar devices and more recently longitudinal tensile strain was demonstrated with nanowire FETs, the effect of radial strain on the carrier transport in nanowires is unknown.

One of the main challenges with studying the impact of radial strain in a nanowire FET is that the gate material needs to be varied to change the strain level. Altering the gate conductor changes the induced strain but also other properties of the device such as the work function. Additionally, the use of different gate materials requires substantial processing development.

SUMMARY

In accordance with an aspect of the invention, an intermediate process device is provided and includes a nanowire connecting first and second silicon-on-insulator (SOI) pads, a gate including a gate conductor surrounding the nanowire and poly-Si surrounding the gate conductor and silicide forming metal disposed to react with the poly-Si to form a fully silicided (FUSI) material to induce radial strain on the nanowire.

In accordance with an aspect of the invention, an intermediate process device is provided and includes first and second pads, a nanowire, formed in a silicon-on-insulator (SOI) layer disposed over a buried oxide (BOX) layer, connecting the first and second pads, a gate surrounding the nanowire and including a dielectric adjacent the nanowire, a gate conductor adjacent the dielectric and poly-Si surrounding the gate conductor and silicide forming metal disposed at least along sidewalls of the poly-Si to react with the poly-Si to form a fully silicided (FUSI) material to induce radial strain in the nanowire.

In accordance with an aspect of the invention, a method to induce radial strain in a field effect transistor (FET) nanowire is provided and includes surrounding the nanowire with a gate conductor and surrounding the gate conductor with poly-Si, and reacting the poly-Si with silicide forming metal deposited thereon to form a fully silicided (FUSI) material to induce radial strain in the nanowire prior to fabrication of source and drain regions relative to the nanowire.

In accordance with another aspect of the invention, a method to induce radial strain in a field effect transistor (FET) nanowire is provided and includes surrounding the nanowire with a gate conductor and surrounding the gate conductor with poly-Si, reacting the poly-Si with silicide forming metal deposited thereon to form a fully silicided (FUSI) material to induce radial strain in the nanowire, forming spacers on opposing sides of the FUSI material, and fabricating source and drain regions relative to the nanowire subsequent to the reacting.

BRIEF DESCRIPTIONS OF THE SEVERAL VIEWS OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other aspects, features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

FIG. **1** is a perspective view of a nanowire under strain;

FIGS. **2**A and **2**B are views of a nanowire extending across a recessed oxide;

FIGS. **3**A and **3**B are views of a reshaped nanowire extending across the recessed oxide;

FIGS. **4**A and **4**B are views of a nanowire and a poly-Si coated with a gate dielectric and partially coated with TaN;

FIGS. **4**C and **4**D are views of the nanowire and the poly-Si fully coated with the gate dielectric and the TaN;

FIG. **5** is a side sectional view of a metallic coating;

FIG. **6** is a side sectional view of a FUSI stressor;

FIG. **7** is a side sectional view of the FUSI stressor of FIG. **6** with spacers;

FIG. **8** is a side sectional view of the FUSI stressor of FIG. **6** with spacers and epitaxy; and

FIG. **9** is a side sectional view of the FUSI stressor of FIG. **6** with spacers and epitaxy and a silicide coating.

DETAILED DESCRIPTION

The present techniques provide a gate-all-around (GAA) nanowire field effect transistor (FET) as well as methods for fabricating the same. In this discussion, reference will be made to various drawings that illustrate embodiments of the present teachings. Since the drawings of the embodiments of the present teachings are provided for illustrative purposes, the structures contained therein are not drawn to scale.

The present methods are described using silicon (Si) nanowires and Si processing. However, the present techniques can also be practiced with other semiconductor materials such as, for example, germanium (Ge) or III-V semiconductors. When non-Si-containing semiconductors are used, the processing steps of the present teachings are basically the same except that growth temperature and dopant species applied are adapted to the specific semiconductor used. Use of Si-containing semiconductor materials such as Si, silicon germanium (SiGe), Si/SiGe, silicon carbide (SiC) or silicon germanium carbide (SiGeC), for example, are preferred however. It is noted that a portion of the nanowires is used herein as the device channel or body.

With reference to FIG. **1**, in an FET with a nanowire channel **10**, it is possible to relatively efficiently induce radial strain ($\Delta r/r$) as well as longitudinal strain ($\Delta L/L$), with r and L being the nanowire's radius and length, respectively, and Δr and ΔL being the change in radius and the change in length, respectively, as a result of stress. The small diameter of the nanowire **11** leads to efficient strain coupling from a stressor with a residual stress, P, such as the material that would normally surround the nanowire **11** that generates a residual stress, C, in the nanowire. While longitudinal strain has been studied in detail in planar devices and, more recently, longitudinal tensile strain was demonstrated with nanowire FETs,